REMARKS

I. Introduction

Claims 2 and 11 have been canceled, without prejudice, and therefore claims 1, 3-10 and 12 are currently pending. Claims 1, 3, 5, 6, 10 and 12 have been amended. The amendments to the claims do not add new matter. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are in allowable condition.

Applicants note with appreciation the acknowledgment of the claim for foreign priority and the indication that all certified copies of the priority documents have been received.

II. Drawings

The drawings were objected to under 37 C.F.R. § 1.83(a). The Office Action states that the steps in Figure 2 lack meaningful labels.

To expedite prosecution, Applicants herein submit a replacement drawing of Figure 2, which now includes descriptive labels for each of the steps. No new matter has been added. Accordingly, withdrawal of the objection to the drawings is respectfully requested.

III. Specification

The Office Action asserts that the Applicants' use of the word "level" (e.g., lines 18-19, page 4 of the specification provides, "The levels present can then be measured") is arbitrary, vague and indefinite. In particular, the Examiner asserts that while "level" is defined as a magnitude according to the IEEE Authoritative Dictionary, it would be impossible for one of ordinary skill in the art at the time the invention was made to make or use any of the teachings associated with the term "level" without stating precisely what parameter the "level" refers to.

Applicants respectfully traverse this objection because it is submitted that those skilled in the art, i.e., familiar with JTAG procedures, would clearly recognize what the "levels present that can be measured" refer to. In this regard,

Applicants note that the specification explains that a predefined test data stream is transmitted across the JTAG interface to the microprocessor or the microcontroller. The levels present can then be measured at the pins of an interface of the microcontroller. It is further stated that the levels present at these pins of the microcontroller's interface are dependent on the test data stream and on the performance reliability of the microcontroller. (Specification, page 4, lines 15-23).

From this description of the specification, it is clear that the "level" refers to a signal level that one of skill in the art would measure at the pins of a microcontroller interface. An attached document found on the Internet at http://www.acculogic.com/Products/BoundaryScanHome.htm explains the boundary scan process of IEEE 1149.1, whereby "test vectors" are enabled onto the device pins to perform various tests. From these test vectors, which represent the test data stream, an output stream results that, as stated, depends on the data stream and the reliability of the tested microcontroller. It is well known to those skilled in the art that a "test vector" refers to a preset digital or analog signal. Those skilled in the art, having some knowledge of the relevant IEEE standards would necessarily know and have ready access to the characteristics of the test vector, e.g., whether the signal is a voltage signal vs. a current signal, or a digital signal vs. an analog signal. Having knowledge of the type of test vector employed, the skilled practitioner would also readily understand whether the output measured at the pins of the microcontroller interface refer to voltage or current levels, since the measured parameter depends on the test vector.

It is therefore respectfully submitted that the phrase "the levels present can then be measured" is clearly understandable to those of skill in the art. Withdrawal of the objection to the specification is therefore respectfully requested.

IV. Objection of Claims 10-12

The Examiner objected to claims 10-12 based on alleged informalities in the claim language. In particular, the Examiner has objected to the term "capable of" in the phrase "a test routine capable of being executed on the at least one

microprocessor" in claim 10. Without passing judgment on the merits of this objection, claim 10 has been amended to recite that "the at least one microprocessor is configured to execute a test routine and includes an arrangement for activating the JTAG interface using the test routine."

With respect to claim 12, the Examiner objects to the term "can be" within the phrase "one of levels present can be measured and defined values can be applied from outside the microcontroller." Without passing judgment on the merits of this objection, claim 12 has been amended to recite that "the microcontroller includes an interface to external devices, the interface enabling output levels present at the interface to be measured and enabling input of defined values by an external device." With regard to the Examiner's comment that the measurement or the application of values from or to the interface does not have to happen, Applicants note that the Examiner is incorrect. In claim 12, the employment of the external device in such actions is not being claimed; rather, claim 12 recites that the microcontoller includes an interface – a structure – that enables external devices to be employed, which is a valid structural limitation.

It is therefore submitted that the amendments to claims 10 and 12 cure the objections to the claims. Withdrawal of the objections to claims 10-12 is accordingly respectfully requested.

V. Rejection of Claims 5 and 12 under 35 U.S.C. § 112, first ¶

Claims 5 and 12 were rejected under 35 U.S.C. § 112, first ¶, as failing to comply with the enablement requirement.

The appropriate standard for enablement established by the Supreme Court is whether any experimentation for practicing the invention is undue or unreasonable. (See MPEP § 2164.01 (citing Mineral Separation v. Hyde, 242 U.S. 261, 270 (1916); In re Wands, 858 F.2d. 731, 737, 8 U.S.P.Q.2d 1400, 1404 (Fed Cir. 1988))). Thus, the enablement test is "whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." (See id. (citing United States v. Teletronics, Inc., 857 F.2d 778, 785, 8 U.S.P.Q.2d 1217, 1223 (Fed. Cir.

1988))).

Similar to the objection to the specification noted above, the Office Action asserts that claims 5 and 12 are non-enabling because one skilled in the art would not be able to practice these claims since the term "level" does not explicitly refer to a particular parameter such as voltage or current. As discussed above, it is submitted that the particular parameter involved would be known to those skilled in the art based upon the type of test vector applied to the microcontroller. Thus, for example, if the test vector is a voltage signal, for which a certain output voltage signal is expected (implying the correct operation of the microcontroller), those skilled in the art would measure voltage levels at the interface. It is again emphasized that the actual physical parameter measured (or applied) depends upon the test routine employed, which information would be readily known and/or available to the skilled practitioner without undue experimentation.

In this regard, it is submitted that, without the Examiner providing any evidence as to the skill level of the practitioners in the relevant art, the Examiner is making unsupported assumptions regarding how those skilled in the art would comprehend the subject matter of the specification and the claims. In particular, the Examiner's contention that the skilled practitioner would not be able to practice the inventions of claims 5 and 12 without further explanation of the term "level" in the claims, i.e., exactly what type of signal is being measured or applied, is clearly insufficient to establish a prima facie case of non-enablement. (See M.P.E.P. § 2164.01(a) (citing In re Wands, 858 F.2d at 737, 8 U.S.P.Q.2d at 1404 and 1407) (stating that the level or ordinary skill in the art must be considered for determining whether a specification satisfies the enablement requirement)).

In light of the fact, inter alia, that the Examiner has failed to show any evidence that there would be undue experimentation in practising the inventions of claims 5 and 12, it is respectfully submitted that claims 5 and 12 are enabled by the specification. Withdrawal of the enablement rejection is therefore respectfully requested.

VI. Rejection of Claims 1-12 under 35 U.S.C. § 112, second ¶

Claims 1-12 were rejected under 35 U.S.C. § 112, second ¶, as being incomplete for omitting essential structural cooperative relationships of elements. In particular, the Examiner asserts that the omitted structural cooperative relationship is the relationship between "a method for activating a microprocessor arranged as part of a microcontroller, within a framework of a boundary scan procedure and IEEE standard 1149" and "a JTAG interface" because, allegedly, "in accordance with" and "according to" do not set forth the relationship required for providing a "method for activating a microprocessor arranged as part of a microcontroller, within a framework of a boundary scan test procedure" given "a test routine that is executable on the microprocessor."

Applicants initially note that the second paragraph of 35 U.S.C. § 112 merely requires that "the claims set out and circumscribe a particular subject matter with a reasonable degree of clarity and particularity." M.P.E.P. § 2173.02 (emphasis added). Claim 1 has been amended to recite a method for activating a microprocessor arranged as a part of a microcontroller within a framework of a boundary scan test procedure as set forth in IEEE standard 1149 using a JTAG interface of the microprocessor, comprising the step of activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and then transmitted to the JTAG interface. Claim 1 recites that the microprocessor is activated using the JTAG interface through the action of executing a test routine and transmitting the test routine to the JTAG interface, indicating the cooperation among the recited elements. It is submitted that claim 1, as amended, sets forth the relationship for the recited method given the test routine with a reasonable degree of clarity and particularity. It is therefore submitted that claim 1 and its dependent claims 3-9 are definite.

Since claim 10 has been amended in an analogous manner to claim 1, it is submitted that claim 10, and claim 12, which depends from claim 10, are also definite.

Withdrawal of the indefiniteness rejection of claims 1-12 is therefore respectfully requested.

VII. Rejection of Claims 1-9 under 35 U.S.C. § 112, second ¶

Claims 1-9 were rejected under 35 U.S.C. § 112, second ¶, as being incomplete for omitting essential structural cooperative relationships of element.

With respect to claim 1, the rejection is substantially similar to the above rejection under § 112, second ¶, so the above response to the prior rejection under § 112, second ¶, applies equally here.

With respect to claim 2, it has been canceled, without prejudice, and thus the rejection is moot with respect to this claim.

With respect to claim 3, it has been amended to recite that the setting operation includes inputting a stipulated test sequence in the test routine to the pins of the JTAG interface, and the reading operation includes reading a sequence of output values at the pins of the JTAG interface corresponding to the stipulated test sequence in the test routine. Since the cooperative relationship among the elements is substantially clear, it is submitted that claim 3 is definite.

With respect to claim 5, it has been amended to recite the step of switching the I/O ports of the microprocessor to transmit the test routine for a predefined duration to output ports and to high. Since the cooperative relationship between the switching of the I/O ports to output ports and the test routine is substantially clear, it is submitted that claim 5 is definite.

With respect to claim 6, it has been amended to recite switching the I/O ports of the microprocessor to input ports to enable reception of values from the pins of the JTAG interface generated by the test routine for a predefined duration and applying defined values to an interface of the microcontroller to transmit the stipulated test sequence to the microcontroller. Since the cooperative relationship among the elements is substantially clear, it is submitted that claim 6 is definite.

In light of the foregoing, it is respectfully submitted that pending claims 1 and 3-9 are definite. Withdrawal of the indefiniteness rejection of claims 1-9 is

accordingly requested.

VIII. Rejections of Claims 5 and 12 under 35 U.S.C. § 112, second ¶

Claims 5 and 12 were rejected under 35 U.S.C. § 112, second ¶, as being indefinite for failing to particularly point out and distinctly claim the invention, and as being incomplete for omitting essential structural cooperative relationships of elements.

Regarding the first cause for rejection, it is submitted that the term "levels" as used in claims 5 and 12 would be reasonably clear to those of skill in the art. As discussed above with respect to the enablement rejection, the skilled practitioner would be apprised of the type of level being measured by virtue of the type of test routine being employed. Thus, the term is not vague and indefinite but draws a clear meaning from the context in which it is used within the claim, and from the unambiguous use of the term within the specification.

Regarding the second cause for rejection, Applicants disagree that the lack of a specific description of the type of physical parameter for which a measurement level is taken amounts to "a gap between the elements." Initially, none of the other elements of claims 5 or 12 are rendered indefinite for the lack of a specific description of the type of physical parameter for which a measurement level is taken, and it is therefore not understood how it constitutes a "gap." Second, as noted above, the Examiner has not substantiated the allegation that those of skill in the art would not readily understand what the "levels" refer to within the claims. Since it is believed that those of skill in the art would, in fact, recognize the meaning of the term "levels," depending on the type of test routine being employed, there is no gap in the claims.

It is therefore respectfully submitted that claims 5 and 12 are definite. Withdrawal of the indefiniteness rejection of these claims is accordingly requested.

IX. Rejection of Claims 1-8 and 10-12 under 35 U.S.C. § 102(b)

Claims 1-8 and 10-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 6,560,740 to Zuraski ("Zuraski").

In order to reject a claim under 35 U.S.C. §102, the Office must demonstrate that each and every limitation is identically disclosed in a single prior art reference. See Scripps Clinic & Research Foundation v. Genentech, Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed.Cir. 1991). The identical invention must be shown in as complete detail as is contained in the claim. MPEP §2131.

Claim 1, as amended, recites the steps of activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and then transmitted to the JTAG interface, wherein I/O ports of the microprocessor are connected to pins of the JTAG interface, and a data-in pin of the JTAG interface is activated using the test routine via the I/O ports. It is submitted that Zuraski does not identically disclose each of these features of claim 1.

Zuraski refers to a boundary scan procedure in which a test control unit configures boundary scan cells to form a serial "scan chain" surrounding a logical element. (Zuraski, col. 7, lines 3-5). Zuraski states that "[i]nput values, **produced by external circuitry**, are shifted through the scan chain, then applied to logic 12." (Zuraski, col. 7, lines 5-7 (emphasis added)).

Zuraski further provides four additional terminals (each at the test control unit (26)) in order to accomplish boundary scan testing including a data input terminal (TDI), a data out terminal (TDO). (Zuraski, col. 7, lines 10-12). It is stated that the data input terminal conveys test input values to the test control unit (26), and that the test control unit (26) in turn provides the input values to the boundary scan cells 26. (Zuraski, col. 7, lines 16-19).

These sections of Zuraski which discuss the boundary scan procedure demonstrate that, during a boundary scan procedure, the input data that is entered to the test control unit (26) does not come from the I/O ports of the microprocessor, but rather, comes from external circuitry. This can also be discerned from Figure 1,

in which the TDI terminal of the test control unit is not coupled to the I/O ports of the microprocessor. Moreover, the Examiner's statement that Zuraski discloses activating the pins of the JTAG interface in accordance with the test routine via the I/O ports is incorrect. In that section, Zuraski states that a BIST (Built-in self-test) -- as opposed to a boundary scan procedure – may be performed following assertion of a RESET signal at an I/O terminal (24).[1] There is no disclosure that the RESET signal has any effect upon the test control unit (26), which provides a JTAG interface.

> The present invention, in contrast, provides:
>
> When PAD [I/O] cells are switched to output mode, they are connected to input pins (e.g. data in (DI)) of the JTAG interface, and test data can be transmitted, via the pins, to the microprocessor or microcontroller.

(Specification, page 4, lines 8-10). This arrangement of connecting an I/O port of the microprocessor to the data-in terminal of the JTAG interface and activating the JTAG interface using a test routine via the I/O port is simply not disclosed or suggested by Zuraski, which instead discloses using external circuitry to provide the input data for the boundary scan procedure.

In summary, while Zuraski refers to using internally (microprocessor) generated and stored test data to perform BIST to functionally test embedded memory units, it does not disclose using such internally generated test data to perform a boundary scan procedure as set forth in IEEE 1149, which, as the name suggests, involves the scanning of cells at the boundary of the microprocessor, rather than embedded memory units. Zuraski therefore does not disclose the claimed invention.

Since Zuraski does not disclose each of the recited features of claim 1, it is respectfully submitted that Zuraski does not anticipate claim 1, or claims 3-8,

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[1]The BIST procedure, as distinct from the boundary scan procedure, tests embedded memory units within a logic unit, while a boundary scan procedure test configures boundary scan cells to form a scan chain surrounding a logic unit. See Zuraski, col. 5, lines 48-55; col. 7, lines 1-9.

which depend from claim 1.

Claim 10 recites a microprocessor configured to execute a test routine and includes an arrangement for activating the JTAG interface using the test routine, the arrangement including PAD cells of the microprocessor and connecting leads from the PAD cells to data-in and data-out pins of the JTAG interface, the PAD cells including an input/output port function. For the reasons stated in connection with claim 1, it is submitted that Zuraski also does not anticipate claim 10, or claim 12, which depends from claim 10.

Withdrawal of the anticipation rejection of claims 1-8 and 10-12 is accordingly requested.

X. Rejection of Claim 9 under 35 U.S.C. § 103(a)

Claim 9 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Zuraski in view of U.S. Patent 5,357432 to Margolis et al. (Margolis).

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Claim 9 depends from, and incorporates the limitations of, claim 1. The Margolis reference merely refers to an automatic guidance control system that includes a microcontroller. It does not in any way refer to a boundary scan procedure according to IEEE 1149, let alone refer to specific ways of implementing such a procedure. As such, Margolis fails to cure the critical deficiencies of the primary Zuraski reference discussed above with respect to claim 1. Therefore, the combination of references relied upon does not disclose or suggest each of features of claim 9, which incorporates the features of claim 1.

Withdrawal of the obviousness rejection of claim 9 is therefore respectfully requested.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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